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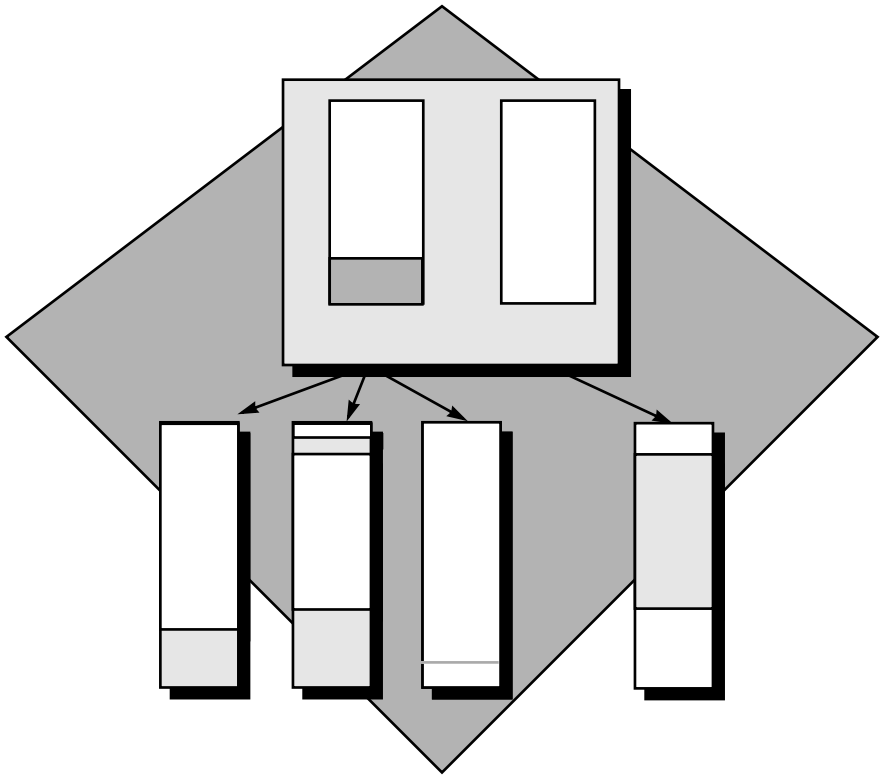
SECTION 3

MEMORY MAPS



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3.1 INTRODUCTION

This section describes in detail the on-chip memories and the internal peripheral memory map of the DSP56602.

3.2 DSP56602 MEMORY MAP DESCRIPTION

The three independent memory spaces of DSP56602: Program, X data, and Y data, are shown in **Figure 3-1**.

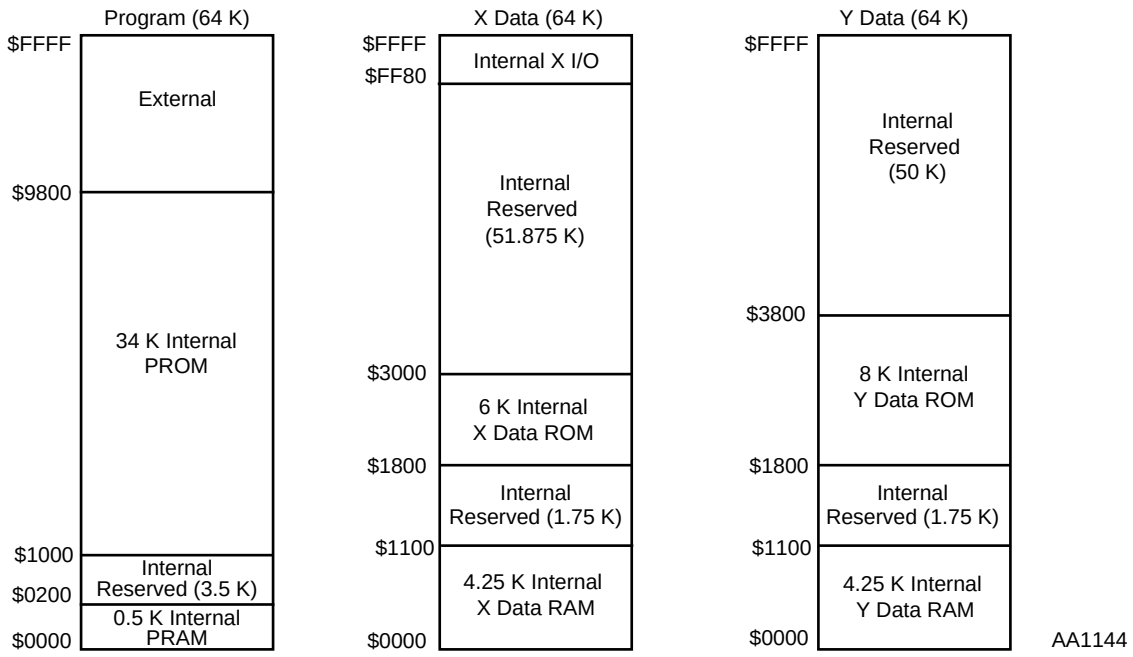

Figure 3-1 DSP56602 Memory Map

The 34 K × 24-bit PROM is factory-programmed to customer specifications. Sample bootstrap ROM code is provided in **Appendix A, Bootstrap Program**.

3.2.1 On-Chip Program Memory

The on-chip program memory consists of two blocks of memory. A 24-bit-wide, high-speed, static memory occupies the lowest locations ($0000–$01FF) in the P memory space. This on-chip Program RAM is organized in two banks, with 256 locations in each bank.

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In addition, a 24-bit-wide block of Program ROM occupies the locations $1000–$97FF. This Program ROM is organized in 136 banks, with 256 locations in each bank. This memory is customer-specified and factory-programmed.

Note: The P memory space located at locations $0200–$0FFF is reserved and should not be accessed.

Program memory from $9800 to $FFFF can be added externally and accessed through the External Memory Interface (Port A).

3.2.2 On-Chip X Data Memory

The on-chip X data RAM is a 16-bit-wide, internal, static memory occupying the lowest locations ($0000–$10FF) in X memory space. The on-chip X data RAM is organized in 17 banks, with 256 locations in each bank.

In addition, a 16-bit-wide block of X data ROM is provided in the locations $1800–$2FFF. This X data ROM is organized in 24 banks, with 256 locations in each bank. This memory is customer-specified and factory-programmed.

The on-chip peripheral registers and some of the core registers occupy the top 128 locations of the X data memory ($FF80–$FFFF). This area is referred to as X I/O space. It can be accessed by the MOVE and the MOVEP instructions, as well as by bit-oriented instructions (such as the BCHG, BCLR, BSET, BTST, BRCLR, BRSET, BSCLR,BSSET, JCLR, JSET, JSCLR, and JSSET instructions).

Note: The X memory spaces located at locations $1100–17FF and $3000–FF7F are reserved and should not be accessed.

3.2.3 On-Chip Y Data Memory

The on-chip Y data RAM is a 16-bit-wide, internal, static memory occupying the lowest locations ($0000–$10FF) in X memory space. The on-chip Y data RAM is organized in 17 banks, with 256 locations in each bank.

In addition, a 16-bit-wide block of Y data ROM is provided in the locations $1800–$37FF. This Y data ROM is organized in 32 banks, with 256 locations in each bank. This memory is customer-specified and factory-programmed.

Note: The Y memory spaces located at locations $1100–17FF and $3800–FFFF are reserved and should not be accessed.

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3.3 MEMORY-MAPPED I/O REGISTERS

All the DSP56602 on-chip peripherals are mapped on the internal X-I/O space, the top 128 locations of the X data memory space. The specific addresses for every on-chip peripheral register or peripheral-mapped register are shown in **Table 3-1**.

Table 3-1 Internal I/O Memory Map

Peripheral	Address	Register Name
PIC	$FFFF	IPR-C—Interrupt Priority Register—Core
	$FFFE	IPR-P—Interrupt Priority Register—Peripheral
PLL	$FFFD	PCTL0—PLL Control Register
	$FFFC	PCTL1—PLL Control Register
OnCE	$FFFB	OGDBR—OnCE GDB Register
BIU	$FFFA	BCR—Bus Control Register
	$FFF9	IDR—ID Register
Patch	$FFF8	PAR0—Patch 0 Register
	$FFF7	PAR1—Patch 1 Register
	$FFF6	PAR2—Patch 2 Register
	$FFF5	PAR3—Patch 3 Register
BPMR	$FFF4	BPMRG—Bus Switch Program Memory Register (24 bits)
	$FFF3	BPMRL—Bus Switch Program Memory Register Low (16 bits)
	$FFF2	BPMRH—Bus Switch Program Memory Register High (16 bits)
(Reserved)	$FFF1 . . . $FFCA	(Reserved)

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Table 3-1 Internal I/O Memory Map (continued)

Peripheral	Address	Register Name
HI08	$FFC9	HDR—HI08 Data Register
	$FFC8	HDDR—HI08 Data Direction Register
	$FFC7	HTX—HI08 Transmit Data Register
	$FFC6	HRX—HI08 Receive Data Register
	$FFC5	HBAR —HI08 Base Address Register
	$FFC4	HPCR—HI08 Port Control Register
	$FFC3	HSR—HI08 Status Register
	$FFC2	HCR—HI08 Control Register
(Reserved)	$FFC1	(Reserved)
	$FFC0	
SSI0	$FFBF	PCRC—SSI 0 Port Control Register
	$FFBE	PRRC—SSI 0 GPIO Direction Register
	$FFBD	PDRC—SSI 0 GPIO Data Register
	$FFBC	TX0—SSI 0 Transmit Data Register
	$FFBB	TSR0—SSI 0 Time Slot Register
	$FFBA	RX0—SSI 0 Receive Data Register
	$FFB9	SSISR0—SSI 0 Status Register
	$FFB8	CRC0—SSI 0 Control Register C
	$FFB7	CRB0—SSI 0 Control Register B
	$FFB6	CRA0—SSI 0 Control Register A
(Reserved)	$FFB5 . . . $FFB0	(Reserved)
SSI1	$FFAF	PCRD—SSI 1 Port Control Register

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Table 3-1 Internal I/O Memory Map (continued)

Peripheral	Address	Register Name
SSI1 (continued)	$FFAE	PRRD—SSI 1 GPIO Direction Register
	$FFAD	PDRD—SSI 1 GPIO Data Register
	$FFAC	TX1—SSI 1 Transmit Data Register
	$FFAB	TSR1—SSI 1 Time Slot Register
	$FFAA	RX1—SSI 1 Receive Data Register
	$FFA9	SSISR1—SSI 1 Status Register
	$FFA8	CRC1—SSI 1 Control Register C
	$FFA7	CRB1—SSI 1 Control Register B
	$FFA6	CRA1—SSI 1 Control Register A
(Reserved)	$FFA5 . . . $FFA0	(Reserved)
GPIO	$FF9F	PCRE—GPIO Port E Control Register
	$FF9E	PRRE—GPIO Port E Direction Register
	$FF9D	PDRE—GPIO Port E Data Register
(Reserved)	$FF9C . . . $FF90	(Reserved)
Triple Timer	$FF8F	TCSR0—Timer 0 Control/Status Register
	$FF8E	TLR0—Timer 0 Load Register
	$FF8D	TCPR0—Timer 0 Compare Register
	$FF8C	TCR0—Timer 0 Count Register
	$FF8B	TCSR1—Timer 1 Control/Status Register
	$FF8A	TLR1—Timer 1 Load Register

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Table 3-1 Internal I/O Memory Map (continued)

Peripheral	Address	Register Name
Triple Timer (continued)	$FF89	TCPR1—Timer 1 Compare Register
	$FF88	TCR1—Timer 1 Count Register
	$FF87	TCSR2—Timer 2 Control/Status Register
	$FF86	TLR2—Timer 2 Load Register
	$FF85	TCPR2—Timer 2 Compare Register
	$FF84	TCR2—Timer 2 Count Register
	$FF83	TPLR—Timer Prescaler Load Register
	$FF82	TPCR—Timer Prescaler Count Register
(Reserved)	$FF81	(Reserved)
	$FF80	

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